MIPS32 4K™ LV (4Kc, TI F731940) Specification Update

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Preface

This document communicates updates to the specifications of the family of MIPS32 4K™ and MIPS64 5K™ Processor Lead Vehicles contained in the document *MIPS 4K/5K™ Lead Vehicle Datasheet*, Ref[1].

There are variations in the characteristics of the Lead Vehicles. These are due to the variations in the type, revision, and configuration of the Lead Vehicle, and they are dependent on the vendor, the process technology, and the production series. Through the on-going validation and characterization of the Lead Vehicles, MIPS identifies updates and additions to the information in the documentation for the Lead Vehicles. The Specification Updates in this document are specific to the

- *MIPS32 4K Processor Lead Vehicle with manufacturing ID TI F731940*.

The Specification Updates can be classified as deviations from the generic specifications, additional information, or defects.

The document is primarily intended for hardware system developers building boards equipped with MIPS32 4K or MIPS64 5K Processor Lead Vehicles.

The document presents additional information and detailed descriptions of defects and deviations from the specifications in the Datasheet. There are sections for updates to the chip pin description, AC & DC specifications, power supply, operating frequency, and other specification updates.

When the Update is a defect, the sections include descriptions of the problem, the implications on the system, a suggested workaround, and a status. The status of a defect will be described by one of the following codes:

Table 1 Status Codes Used in Summary Tables

Code	Description
Open	This issue is under investigation.
Fix	This issue is intended to be fixed in a future version of the component.
Fixed	This issue has been fixed in a previous version.
NoFix	There are no plans to fix this issue.
Doc	The appropriate documents will be updated in the future.

Emphasis of Range Violations and Document Modifications

Throughout the document a shaded field in a table is used to emphasize that this value is deviating from, or violating, the range specified in the Datasheet. Also, modifications of the contents of this document since the previous revision of this document is highlighted by a vertical bar in the margin.

1 Specification Updates to TI F731940

In the following, additional specific information on this particular Lead Vehicle is provided. The information is structured as a set of sub-sections containing specifications that must be present for each Lead Vehicle. These sub-sections are a supplement to the Datasheet and consist of:

- Basic Information
- Supply Voltages
- Test-related Pin-out
- DC Specifications
- AC Specifications
- PLL Connections and Loop Filter

These are followed by a sub-section on Specification Updates that are unique for this Lead Vehicle and are not covered elsewhere. The Updates do have a tracking number prefixed with the letter U (for Update). The following table lists the Updates and their status.

Table 2 Summary of Specification Updates

Update Number	Description	Status
	Note: This table is empty	

1.1 Basic Information

The basic information for the Lead Vehicle is summarized in the following table.

Throughout this document, the newest pin naming style convention has been followed. That is the style where all low-active pins end in “_n” and where the old style suffix “p” has been dropped from all high-active pins.

Table 3 Lead Vehicle Information

Vendor	Texas Instruments
Type	4Kc core
Part ID	TI F731940
Data Cache	4-way, 4 kByte sets, 16 kByte total
Instruction Cache	4-way, 4 kByte sets, 16 kByte total
MMU	TLB with 16 dual entries
EJTAG Support	4 I breaks, 2 D breaks, TAP module
RTL Version	1.1
Static Input Signals to Core: EJ_ManufID[10:0] EJ_PartNumber[15:0] EJ_Version[3:0]	 0x17 0xb31e 1
CP0 PRID Value	0x018001

1.2 Supply Voltages

The Lead Vehicle's three power supply voltages, the I/O power supply, the core power supply, and the PLL power supply (quiet Vss, Vdd) are listed in the following table.

Table 4 Supply Voltages

VDD (I/O buffers)	CVDD (Core)	VDDA (PLL supply)
3.3V +/-10%	1.8V +/-10%	3.3V +/-10%

There are no special requirements to the order in which the power supplies are powering up, or down.

1.3 Test-related Pin-out

The following table lists deviations and additions to the functional pin descriptions given in the Datasheet. Table 5 shows the format of the implementor test pins. The test pins are only for internal undocumented use. The input pins should be left de-asserted.

Table 5 Test Pin Descriptions

Test mode pins (implementor use only)			
Pin name	**Type**	**Control Pin**	**Description**
TIN[0]	I	TSM	Non-public. For production test.
TIN[1]	I	TSM	Non-public. For production test.
TIN[2]	I		Non-public. For production test.
TIN[3]	I		Non-public. For production test.
TIN_N[0]	I	TSM	Non-public. For production test.
TIN_N[1]	I	TSM	Non-public. For production test.
TIN_N[2]	I	TSM	Non-public. For production test.
TIN_N[3]	I	TSM	Non-public. For production test.
TOUT[0]	O		Non-public. For production test.
TOUT[1]	O		Non-public. For production test.
TOUT[2]	O		Non-public. For production test.
TOUT[3]	O		Non-public. For production test.

1.4 DC Specifications

The pad drivers on this Lead Vehicle are all from the LVCMOS Standard Interface family in the TI ASIC cell library GS20. The following information is reprinted with permission from Texas Instruments.

Table 6 Recommended Operating Conditions

Parameter	Description	Min	Nom	Max
VDD	I/O buffer supply voltage	3.0 V	3.3 V	3.6 V
V_I	Input voltage	0 V		VDD
V_O	Output voltage	0 V		VDD
V_{IH}	High-level input voltage	0.7 VDD		
V_{IL}	Low-level input voltage	0 V		0.3 VDD

Table 7 Electrical Characteristics

Parameter	Condition	Min	Max
V_{OH}	I_O = rated	2.4 V	
V_{OL}	I_O = rated		0.22 VDD
I_{IH}	$V_I = V_I$ max		+/- 1 µA
I_{IL}	$V_I = V_I$ max		+/- 1 µA
I_{OZ}	VDD = 3.6 V		+/- 20 µA

The input drivers are all of the same type, IDG04, and the output drivers are of type OUI43 and OUK83. The following table lists the loading factors for all driver types. For the output drivers the rated I_O is included, as well. The load factors (i.e. the capacitance on the input pins of the input drivers, and the capacitance on the output of the output driver) are the typical values for a nominal process under nominal conditions at VDD = 3.3 V.

Table 8 Driver Characteristics

Driver	I/O	Load Factor	I_O
IDG04	I	1.494 pF	
OUI43	O	2.522 pF	4 mA[a] (TBD)
OUK83	O	2.825 pF	8 mA[b] (TBD)

a. The rated I_O is still to be determined. It is recommended not to go beyond 4 mA for this driver.

b. The rated I_O is still to be determined. It is recommended not to go beyond 8 mA for this driver.

1.5 AC Specifications

This section shows any deviations of the AC specifications from the corresponding descriptions in the Datasheet. All violations of the previous described value ranges are highlighted with a shaded background in the table. First, an overview of the clock AC specifications is provided. Then, tables for the AC requirements of the pins are presented.

1.5.1 Clock Signals

The table below shows the frequency and duty cycle ranges for all the input clock pins in the Lead Vehicle. The duty cycle is here specified as the percentage of the cycle where the phase is high.

Note that in the SysAD64 mode with the PLL enabled, the internal processor core frequency is twice the frequency of the external GCLK input pin.

Table 9 Clocking Frequency and Duty Cycle Range

Pin, Mode	Min	Max
Core clock frequency range.	0 MHz	80 MHz
PLL output frequency range	50 MHz	210 MHz
GCLK frequency range, SysAD64 (PLL enabled)	25 MHz	40 MHz
GCLK duty cycle, SysAD64 (PLL enabled)	45	55
GCLK frequency range, core bond-out (PLL disabled)	0 MHz	66 MHz
GCLK duty cycle, core bond-out (PLL disabled)	40	60
ETCK frequency range	0 MHz	40 MHz
ETCK duty cycle	min. 10 ns high, and min. 10 ns low	

The silicon works within the above minimum specifications. For additional information regarding characterization data, please contact the silicon manufacturer (TI) directly.

1.5.2 Other Functional Pins

The following three tables list the AC/DC pin specifications. Values that violates the ranges specified in the Datasheet are highlighted using a shaded background.

Table 10 AC/DC Pin Specs for Shared Function Pins

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
GCLK	I	IDG04						
GCLKB	O	OUI43	25	GCLK				
GRST2_N	I	IDG04		DC				
GBYPASS	I	IDG04		DC				
GMULT[1:0]	I	IDG04		DC				
CBIGEN	I	IDG04		DC				
CTIMER5	I	IDG04		DC				
CSYSAD	I	IDG04		DC				
CPIPEWR	I	IDG04		DC				
C4WBLK	I	IDG04		DC				

Table 10 AC/DC Pin Specs for Shared Function Pins (Continued)

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
ETCK	I	IDG04						
ETMS	I	IDG04		DC				
ETDI	I	IDG04		ETCK			4	1
ETDO	O (3S)	OUI43	25	ETCK[a]	2	9.1		
ETRST_N	I	IDG04		DC				
EDINT	I	IDG04		ASYNC				
ERES[11:0]	O	OUK83	50					
TSE	I	IDG04		DC				
TSM	I	IDG04		DC				
TSI	I	IDG04		DC				
TSO	O	OUK83	25					
TIN[3:0]	I	IDG04		DC				
TIN_N[3:0]	I	IDG04		DC				
TOUT[3:0]	O	OUK83	25					
MBUS	I	IDG04		DC				
MINP[3:0]	I	IDG04		DC				
MINP_N[3:0]	I	IDG04		DC				

a. The ETDO output timing is specified relative to the negative edge of ETCK.

Table 11 AC/DC Pin Specs for SysAD64 Mode

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
GRST_N	I	IDG04		ASYNC				
SSYSAD[63:0]	I/O	OUI43 IDG04	25	GCLK	2	10.7	3.0	0
SSYSCMD[8:0]	I/O	OUI43 IDG04	25	GCLK	2	10.0	2.3	0
SSYSADC[7:0]	I/O	OUI43 IDG04	25	GCLK	2	10.0	2.9	0

Table 11 AC/DC Pin Specs for SysAD64 Mode (Continued)

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
SSYSCMDP	I/O	OUI43 IDG04	25	GCLK	1.9	9.4	2.6	0
SRDRDY_N	I	IDG04		GCLK			2	0
SWRRDY_N	I	IDG04		GCLK			2	0
SVALIDIN_N	I	IDG04		GCLK			2	0
SVALIDOUT_N	O	OUI43	25	GCLK	2	8.7		
SEXTRQST_N	I	IDG04		GCLK			2	0
SRELEASE_N	O	OUI43	25	GCLK	2	8.8		
IINT_N[5:0]	I	IDG04		ASYNC				
INMI_N	I	IDG04		ASYNC				

Table 12 AC/DC Pin Specs for Core Bond-out Mode

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
EB_A[35:2]	O	OUI43	25	GCLK	2.6	14.9		
EB_WData[63:0]	O	OUI43	25	GCLK	3	14.8		
EB_RData[63:0]	I	IDG04		GCLK			6	0
EB_BE[7:0]	O	OUI43	25	GCLK	3	15.0		
EB_AValid	O	OUI43	25	GCLK	3	15.0		
EB_Write	O	OUI43	25	GCLK	3	14.9		
EB_Instr	O	OUI43	25	GCLK	3	14.8		
EB_Burst	O	OUI43	25	GCLK	3	14.7		
EB_BFirst	O	OUI43	25	GCLK	3	14.6		
EB_BLast	O	OUI43	25	GCLK	3	14.7		
EB_BLen[1:0]	O	OUI43	25	GCLK	3	10		
EB_ARdy	I	IDG04		GCLK			6	0
EB_RdVal	I	IDG04		GCLK			6	0
EB_WDRdy	I	IDG04		GCLK			6	0
EB_RBErr	I	IDG04		GCLK			6	0
EB_WBErr	I	IDG04		GCLK			6	0
EB_WWBE	O	OUI43	25	GCLK	3	14.7		

Table 12 AC/DC Pin Specs for Core Bond-out Mode (Continued)

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
EB_EWBE	I	IDG04		GCLK			6	0
EB_SBlock	I	IDG04		GCLK			6	0
SI_Int[5:0]	I	IDG04		GCLK			6	0
SI_NMI	I	IDG04		GCLK			6	0
SI_ColdReset	I	IDG04		GCLK			6	5.4
SI_Reset	I	IDG04		GCLK			6	0
SI_MergeMode[1:0]	I	IDG04		GCLK			6	0
SI_RP	O	OUI43	25	GCLK	3	14.5		
SI_Sleep	O	OUI43	25	GCLK	3	14.1		
SI_TimerInt	O	OUI43	25	GCLK	3	13.7		
SI_ERL	O	OUI43	25	GCLK	3	14.2		
SI_EXL	O	OUI43	25	GCLK	3	14.8		
EJ_PerRst	O	OUI43	25	GCLK	3	10		
EJ_PrRst	O	OUI43	25	GCLK	3	10		
EJ_SRstE	O	OUI43	25	GCLK	3	10		
EJ_DebugM[a]	O	OUI43	25	GCLK	N/A	N/A		
PM_DCacheHit	O	OUK83	25	GCLK	3	12.6		
PM_DCacheMiss	O	OUK83	25	GCLK	3	12.6		
PM_ICacheHit	O	OUK83	25	GCLK	3	12.6		
PM_ICacheMiss	O	OUK83	25	GCLK	3	12.6		
PM_InstnComplete	O	OUK83	25	GCLK	3	12.6		
PM_ITLBHit	O	OUK83	25	GCLK	3	12.6		
PM_ITLBMiss	O	OUK83	25	GCLK	3	12.6		
PM_JTLBHit	O	OUK83	25	GCLK	3	12.6		
PM_JTLBMiss	O	OUK83	25	GCLK	3	12.6		
PM_WTBMerge	O	OUK83	25	GCLK	3	12.6		
PM_WTBNoMerge	O	OUK83	25	GCLK	3	12.6		
PM_DTLBHit[b]	O	OUK83	25	GCLK	N/A	N/A		

Table 12 AC/DC Pin Specs for Core Bond-out Mode (Continued)

Pin name	Type	Buffer Type	Extern load [pF]	Reference Clock	Clk2out min [ns]	Clk2out max [ns]	Input setup [ns]	Input hold [ns]
PM_DTLBMiss[b]	O	OUK83	25	GCLK	N/A	N/A		

a. The EJ_DebugM signal isn't driven on this LV.

b. The PM_DTLBHit and PM_DTLBMiss pins are not driven on this device, as it does not contain a DTLB. The value on the pins is therefore undefined.

1.6 PLL Connections and Loop Filter

The following table shows the pin-out for the 6 analog connections to the PLL (quiet supplies, optional loop filter etc.). LF in the table is the loop filter connection for the PLL. The specifics are described below.

Table 13 PLL Pin-out

B13	D13	A13	C14	B12	C13
NC	NC	VSSA	LF	VDDA	NC

This Lead Vehicle uses an external loop filter. The figure below shows the filter circuit, and the table shows the component values. All components should be +/- 5% or better.

Table 14 PLL Loop Filter Component Values

Value of R1	Value of C1	Value of C2
62 ohm	16 nF	300 pF

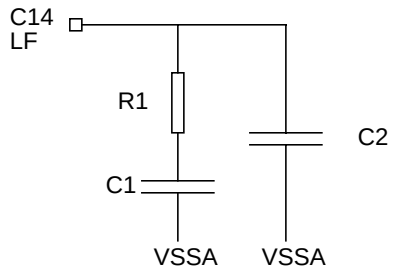

Figure 1 Loop Filter Schematic

For this type of loop filter, it is the R1,C1 which are the critical components. These two components must have the shortest possible trace lengths on the PCB connecting to the LV. C2 is also critical, but not as much as R1,C1.

2 Software-configurable Features of the 4K Core in the Lead Vehicle

This Lead Vehicle allows the manipulation of some otherwise read-only bits in the CP0 Config register. The features that can be modified are the cache configuration bits in the Config Select 1 Register. The ability to change these features in software enables evaluation and benchmarking of the effect of different caches sizes and organizations beyond the default cache implemented on this Lead Vehicle.

The features described in this section are present specifically to support configuration testing of the core in a Lead Vehicle, and are not supported in any other environment. Attempting to use these features outside of the scope of a Lead Vehicle is a violation of the MIPS Architecture, and may cause unpredictable operation of the processor.

2.1 Config Register Format — Select 0

31	30		28	27		25	24			21	20	19	18	17	16	15	14	13	12		10	9		7	6			3	2		0
M	K23			KU			R				MDU	**WC**	MM		BM	BE	AT		AR			MT			0				K0		

The format of Config (Select 0) Register is shown above and the bit fields are described in Table 15. Most of the fields are identical to the description of this register in the *MIPS32 4K™ Processor Core Family Software User's Manual*, but the whole register is shown here for completeness. The modified fields relevant to the software configuration features are highlighted in bold type in the tables. Here is an overview of the modified fields in this register:

- WC (bit 19): This new read/write bit is a write enable for the software-configurable features within the Config Register available on this Lead Vehicle. It can be written to either 1 or 0, but is initialized to 0. When this field is set to 1, the cache configuration fields in Config Select 1 become writeable.

Table 15 Config Register Field Descriptions

Fields		Description	Read/ Write	Reset State
Name	**Bit(s)**			
M	31	This bit is hardwired to '1' to indicate the presence of the Config register.	R	Preset
K23	30:28	This field controls the cacheability of the kseg2 and kseg3 address segments in BAT implementations. This field is valid in the 4Kp and 4Km processor and is reserved in the 4Kc processor. Refer to Table 16 for the field encoding.		
KU	27:25	This field controls the cacheability of the kuseg and useg address segments in BAT implementations. This field is valid in the 4Kp and 4Km processor and is reserved in the 4Kc processor. Refer to Table 16 for the field encoding.		
R	24:21	Reserved. Returns a zero value when read.	R	0
MDU	20	This bit indicates the MDU type. 0 = Fast Multiplier Array (4Kc and 4Km) 1 = Iterative multiplier (4Kp)		
WC	**19**	**Write enable bit for cache configuration bits in Config Select 1.**	**R/W**	**0**

Table 15 Config Register Field Descriptions (Continued)

Fields		Description	Read/ Write	Reset State
Name	Bit(s)			
MM	18:17	This field contains the merge mode for the 32-byte collapsing write buffer: 00 = No Merging 01 = SysAD Valid merging 10 = Full merging 11 = Reserved	R	Preset
BM	16	Burst order. This bit is always zero to indicate sequential burst mode.	R	0
BE	15	Indicates the endian mode in which the processor is running: 0: Little endian 1: Big endian	R	Preset or Externally Set
AT	14:13	Architecture type implemented by the processor. This field is always 00 to indicate MIPS32.	R	Preset
AR	12:10	Architecture revision level. This field is always 000 to indicate revision 1. 0: Revision 1 1-7: Reserved	R	Preset
MT	9:7	MMU Type: 1: Standard TLB (4Kc) 3: Fixed Mapping (4Kp, 4Km) 0, 2, 4-7: Reserved	R	Preset
0	6:3	Must be written as zero; returns zero on read.	0	0
K0	2:0	Kseg0 coherency algorithm. Refer to Table 16 for the field encoding.	R/W	Undefined

Table 16 Cache Coherency Attributes

C(2:0) Value	Cache Coherency Attribute
0, 1, 3*, 4, 5, 6	Cacheable, noncoherent, write-through, no write allocate
2*, 7	Uncached
* These two values are required by the MIPS32 architecture. In the 4Kc and 4Kp processor cores, all other values are not used. For example, values 0, 1, 4, 5 and 6 are not used and are mapped to 3. The value 7 is not used and is mapped to 2. Note that these values do have meaning in other MIPS Technologies processor implementations. Refer to the MIPS32 specification for more information.	

2.2 Config1 Register Format — Select 1

31	30					25	24		22	21	20	19	18	17	16	15	14	13	12		10	9		7	6	5	4	3	2	1	0
0	MMU Size						IS			IL			IA			DS			DL			DA			0		PC	WR	CA	EP	FP	

The format of Config (Select 1) Register is shown above and the bit fields are described in Table 17. Most of the fields are identical to the description of this register in the *MIPS32 4K™ Processor Core Family Software User's Manual* but

the whole register is shown here for completeness. The modified fields relevant to the software configuration features are highlighted in bold type in the tables. Here is an overview of the modified fields in this register:

- The instruction cache configuration fields (IS, IL and IA) and the data cache configuration fields (DS, DL and DA) which are otherwise read-only become writeable when the WC bit in the Config Select 0 register is set. Note that only certain values for these fields are legal, while other encodings are reserved.

Table 17 Config1 Register Field Descriptions — Select 1

Fields		Description	Read/ Write	Reset State
Name	**Bit(s)**			
0	31	This bit is reserved to and must be read or written as zero.	R	Preset
MMU Size	30:25	This field contains the number of entries in the TLB minus one. The field is read as 15 decimal in the 4Kc processor and as 0 decimal in the 4Kp and 4Km processors.	R	Preset
IS	**24:22**	This field contains the number of instruction cache sets per way. Three options are available in both cores. All others values are reserved: 0x0: 64 0x1: 128 0x2: 256 0x3 - 0x7: Reserved	**R/W**	**Preset**
IL	**21:19**	This field contains the instruction cache line size. If an instruction cache is present, it must contain a fixed line size of 16 bytes. 0x0: No Icache present 0x3: 16 bytes 0x1, 0x2, 0x4 - 0x7: Reserved	**R/W**	**Preset**
IA	**18:16**	This field contains the level of instruction cache associativity. 0x0: Direct mapped 0x1: 2-way 0x2: 3-way 0x3: 4-way 0x4 - 0x7: Reserved	**R/W**	**Preset**
DS	**15:13**	This field contains the number of data cache sets per way: 0x0: 64 0x1: 128 0x2: 256 0x3 - 0x7: Reserved	**R/W**	**Preset**
DL	**12:10**	This field contains the data cache line size. If a data cache is present, it must contain a line size of 16 bytes. 0x0: No Dcache present 0x3: 16 bytes 0x1, 0x2, 0x4 - 0x7: Reserved	**R/W**	**Preset**
DA	**9:7**	**This field contains the type of set associativity for the data cache:** **0x0: Direct mapped** **0x1: 2-way** **0x2: 3-way** **0x3: 4-way** **0x4 - 0x7: Reserved**	**R/W**	**Preset**
0	6:5	Must be written as zero; returns zero on read.	0	0

Table 17 Config1 Register Field Descriptions — Select 1 (Continued)

Fields		Description	Read/ Write	Reset State
Name	Bit(s)			
PC	4	Performance Counter registers implemented. Always a 0 since the cores do not implement any.	R	0
WR	3	Watch registers implemented. This bit is always read as 1 since the cores each contain one pair of Watch registers.	R	1
CA	2	Code compression (MIPS16) implemented. This bit is always read as 0 because MIPS16 is not supported.	R	0
EP	1	EJTAG present: This bit is always set to indicate that the core implements EJTAG.	R	1
FP	0	FPU implemented. This bit is always zero since the core does not contain a floating point unit.	R	0

2.3 Cache Configuration in Config Select 1

The cache configuration bits in the Config Select 1 Register can be written to modify the default cache size and organization.

Here is the sequence which must be used to accomplish a change in the cache configuration bits. This sequence should be executed in uncacheable space to avoid unpredictable behavior.

1. MTC0 instruction to set WC field in Config Select 0.
2. One or more additional MTC0 instructions to write the instruction and data cache configuration bits in Config Select 1 to their desired values.

Here are some additional considerations to keep in mind:

- Obviously, you cannot select a larger cache size or organization than the largest size present on the 4K core in the Lead Vehicle.
- The instruction and data caches can be configured independently.
- It is possible to disable a cache by setting the line size field (IL or DL) to zero.
- Only certain values for the cache configuration fields are legal in the 4K processor core, as detailed in Table 17.
- If you downsize or disable a cache with this method, only new line allocations are disabled. Loads or stores to “old” entries will still hit, even if they are in that part of the cache which has been downsized. If you do not desire this behavior, then you should initialize all the tag entries for the maximum cache configuration to be invalid before you select your new cache configuration.

Appendices

A References

[1] MIPS 4K/5K™ Lead Vehicle Datasheet
Document no: MD00001
MIPS Technologies, Inc.

B Revision History

Table 2-1

Revision	Date	Description
01.00	Jan. 7, 2000	Initial Release.
01.01	Feb. 4, 2000	Included processor core type in document title
01.02	Feb. 7, 2000	Added description of CP0 Configuration Register support for software modification of cache size and organization.
01.03	Mar. 10, 2000	• Updated load factor value for OUK83 output driver in Table 8. • Modified disclaimer regarding use of software-configurable features.
01.04	Mar. 27, 2000	• Added comment regarding characterization data in Table 9.
01.05	May 26, 2000	• Updated ETDO pin timing in Table 10 to show that max clock-to-out timing does not meet Datasheet spec. • Updated copyright notice and document footer. • Converted note about PM_DTLB* signals to a footnote in Table 12.
01.06	May 31, 2000	• Added standard trademark notices.
01.07	Feb. 8, 2001	• Updated to new document template.
01.08	Aug. 1, 2001	• Correct Read/Write status for Config0.MT field in Table 15; it is a read-only field.